This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A processor unit system for a shared-memory computer comprising:

a processor unit;

a local memory system executing a protocol to share data with at least one other processor unit;

a conflicts resolution circuit executing a hardware program to:

(i) detect a critical section in an executing program and begin speculative execution of the critical section without acquisition of a lock;

(ii) in the event of a conflict with another processor unit executing the critical section and needing to write to data within the critical section, establishing a priority between the processor units and another processor unit to resolve the conflict without acquisition of the lock.

2. (Currently Amended) The processor unit system of claim 1 further including:

a clock with a globally unique clock value;

and where the conflicts resolution circuit establishes a priority between the processor units and another processor unit by:

(a) time stamping requests for data sent by a first processor unit to other processor units with the globally unique clock value ;

(b) releasing owned data that is requested by a second processor unit, if the second processor is making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the first processor unit;

(c) deferring release of owned data that is requested by the second processor unit, if the second processor is making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the first processor unit.

3. (Previously Presented) The processor unit system of claim 2 wherein the conflicts resolution circuit executes hardware program step (ii) only during execution of a critical section.

4. (Previously Presented) The processor unit system of claim 2 wherein the processor unit system uses a protocol of the local memory during execution of a section of the program that is not a critical section.

5. (Previously Presented) The processor unit system of claim 4 wherein the protocol of the local memory is a cache coherence protocol.

6. (Currently Amended) The processor unit system of claim 2 wherein the clock with a globally unique clock value ~~provides~~ includes a time variant field and a static processor-unit-dependant field.

7. (Previously Presented) The processor unit system of claim 2 wherein the clock with a globally unique clock value is a counter updated after executions by the processor unit of a critical section of a program subject to a lock.

8. (Previously Presented) The processor unit system of claim 7 wherein the counter sets itself to a higher number on updating.

9. (Previously Presented) The processor unit system of claim 8 wherein the counter sets itself to the time stamp of the request of the second processor unit when the release of data is deferred because the time stamp of the request of the second processor unit is later.

10. (Previously Presented) The processor unit system of claim 2 further including buffer memory storing a deferred request of the second processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

(d) read buffered deferred requests at a time after a deferring to release data to the second processor unit.

11. (Previously Presented) The processor unit system of claim 10 further including:

a critical section detection circuit detecting the start and end of execution by the processor of a critical section of a program subject to a lock; and

wherein the later time is the completion of a critical section.

12. (Previously Presented) The processor unit system of claim 2 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to the second processor unit when the request by the second processor unit is deferred based on its time stamp.

13. (Previously Presented) The processor unit system of claim 2 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to the second processor unit when the request by the second processor unit is deferred because the requested data is not available.

14. (Previously Presented) The processor unit system of claim 13 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a probe message to a third processor unit containing a time stamp of the request of the second processor unit receiving the marker message.

15. (Previously Presented) The processor unit of system claim 1 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) respond to a probe message from a second processor unit that has sent the processor unit a marker message indicating that a request by the processor unit has been deferred, the probe message indicating a time stamp of a third processor unit earlier than the time stamp of the request used by processor unit to acquire that data, the probe message being from a third processor unit requesting the data from the second processor unit.

16. (Previously Presented) The processor unit system of claim 1 further including:

a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock;

(ii) speculatively execute the critical section without acquiring the lock;

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit; and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section.

17. (Previously Presented) The processor unit system of claim 16 wherein the conflict resolution circuit allows continued speculative execution of the critical section when the conflict is resolved by deferring the release of the data in hardware program step (iii).

18. (Previously Presented) The processor unit system of claim 16 wherein the conflict resolution circuit causes a ceasing of the speculative execution of the critical section when the conflict is resolved by releasing the data in hardware program step (iii).

19. (Previously Presented) The processor unit system of claim 16 further including buffer memory storing deferred requests from the second processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a later time to release data to the second processor unit; and

(v) cease the speculative execution of the critical section when buffer memory is exhausted.

20. (Previously Presented) The processor unit system of claim 16 including buffer memory storing the results of speculative execution; and

wherein the lock elision circuit further executes the hardware program to: (iv) cease the speculative execution of the critical section when buffer memory is exhausted.

21. (Previously Presented) A processor unit system comprising: a plurality of processor units having:

a processor unit;

a local memory system executing a protocol to share data with at least one other processor unit;

a clock with a globally unique clock value;

a conflicts resolution circuit executing a hardware program to:

(i) time stamp requests for data sent by a first processor unit to other processor units with a value of the clock with a globally unique clock value;

(ii) release owned data that is requested by a second processor unit, if the second processor is making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the first processor unit;

(iii) defer release of owned data that is requested by a second processor unit, if the second processor is making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the first processor unit.

22. (Previously Presented) A method of operating a set of processor units for a shared-memory computer comprising the steps of:

(a) generating on each processor unit a clock with a globally unique clock value;

(b) time stamping all requests for data sent by a first processor unit to other processor units with a value of the clock with a globally unique clock value;

(c) releasing owned data that is requested by a second processor unit, if the second processor is making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the first processor unit;; and

(d) deferring release of owned data that is requested by a second processor unit, if the second processor is making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the first processor unit.

23. (Original) A processor unit for a shared-memory computer comprising: a processor;

a local memory system executing a protocol to share data with at least one other processor unit;

a conflicts resolution circuit executing a hardware program to resolve conflicts between different processor units;

a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock;

(ii) speculatively execute the critical section without acquiring the

lock;

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit; and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section.